

Remarks

This is in response to the Office Action mailed on July 31, 2003. Claims 1-4 have been amended, support for the amendments to claim 1 being found, for example, at Figures 3 and 4 and page 4, lines 25-34 and page 5, lines 14-18 of the present application. Claims 5 and 6 have been added. Support for claim 5 can be found, for example, at Figure 5 and page 5, lines 24-30, and support for claim 6 can be found, for example, at Figures 3 and 4 and page 4, lines 25-34 and page 5, lines 14-18 of the application. Claims 1-6 remain pending. Reconsideration and allowance are respectfully requested.

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchida, U.S. Patent No. 6,430,735, in view of Fujima, U.S. Patent No. 5,682,105. This rejection is respectfully traversed, to the extent it is maintained.

Claim 1 is directed to a LSI layout method for a LSI design. Claim 1 recites, among other limitations, providing a power supply capacitor cell in combination with a corresponding logic gate cell, and arranging the power supply capacitor cell in a vicinity of the logic gate cell.

The specification of the present application defines the term "vicinity" as follows.

Here, the term "vicinity" indicates that the power supply capacitor standard cells 22 are placed adjacent to the respective logic gate standard cells 21, which are used for driving load, and that they are arranged on the same power supply lines. Therefore, when the power supply capacitor standard cells are arranged on different power supply lines, regardless of the closeness of both cells, it is not regarded as being placed in the "vicinity".

Application, page 4, lines 29-34. Therefore, the term "vicinity" is used to indicate that the power supply capacitor cells are positioned specifically (e.g., on the same power supply line) with respect to the logic gate cells.

A LSI layout method performed as recited by claim 1 is advantageous, for example, because a reduction in power supply noise due to an inductance component around the power supply line can be realized because the power supply capacitor cell is provided in combination with the specific logic gate cell. See, e.g., page 3, lines 13-18 of the application.

In Uchida, the power supply capacitor cell 18 is arranged in regions such as under vertical wiring 12 between horizontal direction wirings 10 and 11, between vertical direction wirings 12 and 13 and between direction wirings 10 and 11, or at an unused region 15 where a function block 17 is not arranged. See Figures 1, 2, and 7, of Uchida.

The rejection cites column 1, lines 30-35 of Uchida as disclosing placing of capacitors near logic gates. This characterization of Uchida is respectfully traversed. This section of the background of Uchida states the following.

Referring FIG. 8, in conventional LSI, in order to avoid the occurrence of a situation where an on-chip capacitor hinders the disposition of the wirings or limits the arrangement of function blocks, the on-chip capacitor has not been disposed near the transistors causing the ground-bounce. Instead of near the transistors, the in-chip capacitor has been disposed in a spot such as a unused area 43 in an internal region 41 in the LSI where no function block is arranged, a boundary area 44 between the internal region 41 and an Input-Output (I/O) region 42, and a unused area 45 in the I/O region 42 where no I/O buffer is arranged.

Uchida, column 1, lines 27-38 (underline added). Therefore, this section of Uchida simply discloses the positioning of a capacitor with respect to transistors on the LSI. Specifically, this section discloses that the capacitor should not be positioned near the transistors.

Therefore, Uchida fails to disclose positioning a power supply capacitor cell in combination with a logic gate cell, and arranging the power supply capacitor cell in a vicinity of the logic gate cell, as recited by claim 1. Consequently, unlike the configuration recited by claim 1, the power supply capacitor cell 18 disclosed by Uchida does not function to reduce a power supply noise due to an inductance component around the power supply line.

Fujima fails to remedy the shortcomings of Uchida noted above.

For at least these reasons, claim 1 and claims 2-4 that depend therefrom should be allowable. Reconsideration and allowance are respectfully requested.

Claim 5 depends from claim 1 and should therefore be allowable for at least the same reasons as those provided above with respect to claim 1. Consideration and allowance are respectfully requested.

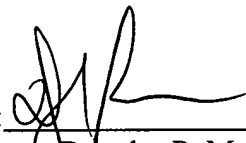
Claim 6 is similar to claim 1, except that claim 6 recites that the power supply capacitor cell is arranged adjacent to the logic gate cell. For similar reasons to those noted above with respect to claim 1, Uchida fails to disclose or suggest arranging the power supply capacitor cell adjacent to the logic gate cell, as recited by claim 6.

Consequently, claim 6 should be allowable over the cited art for at least the same reasons as those provided above with respect to claim 1. Consideration and allowance of claim 6 are respectfully requested.

In view of the above, favorable consideration of claims 1-6 in the form of a Notice of Allowance is requested. The Examiner is invited to contact the undersigned at (612) 371-5237 with any questions regarding this application.

Respectfully submitted,
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